IN THE SPECIFICATION

Please amend the application as follows:

Please add the following paragraph at page 1, after the title:

This application is a continuation of U.S. Patent Application Serial 09/317,442, filed May 24, 1999, which is incorporated herein by reference.

The paragraph beginning at page 10, line 10 is amended as follows:

Although, in the example, the master initiates the transfer of data to memory 103, most of the necessary data command structures are contained in a portion of the memory space of memory 103. So, for example, if there is a command block that instructs the transfer of a data block out ~~wire 17~~ to a master on an ethernet card (i.e., to transfer a block of data and move it onto a local area network) or to receive an incoming packet, the command blocks and the data block are usually contained in the memory space of memory 103.

The paragraph beginning at page 11, line 10 is amended as follows:

The prefetching utilized in the example embodiment of the invention is based on the actual results of past I/O read options to determine whether chipset 101 or MIOC 201 should prefetch or not. The preferred state machine shown in Fig. 5 has four different states. In the top two (501, 502) of the four states, prefetching is carried out, and in the other bottom two (503, 504) of the four states, prefetching is not carried out. The state machine need not be that shown in Fig. [4] 5, but there is in any event a prefetch circuit which does not prefetch until it determines that prefetching will be successful. Once prefetching is successful and is consistently successful, then the prefetch circuit biases itself toward prefetching by using the top state 501. Once prefetching starts to not be so successful, it falls back into a prefetch or not prefetch condition 502, where if it fails the next time, it will quit prefetching and it if it works the next time, it will resume prefetching. Conversely, if prefetching is unsuccessful and is consistently

unsuccessful, then the prefetch circuit biases itself toward not prefetching by using the bottom state 504. Once prefetching would be successful, it rises into a prefetch or not prefetch condition state 503, where if it works the next time, it will prefetch and if it fails the next time, it will discontinue prefetching. This process is generally referred to as tracking.

The paragraph beginning at page 19, line 8 is amended as follows:

This hardware may advantageously be combined in the hardware of MIOC 201 with ~~the~~ a moving average measurement circuit ~~of my previous application incorporated by reference above~~. However, simpler embodiments of the invention are preferred which use a binary model based on the success or failure of previous prefetch decisions. Such a simpler embodiment can be implemented by a comparison between the last address saved in the table shown in Fig. 6 and the new request address. Either prefetch works because there is an exact match or the new request address is within a prefetch range (for example, if four lines are prefetched, then the requested address is one of those four lines). The result of the comparison is used to update the state machine and the table shown logically in Fig. 6.